

**G2X8**

***Disclaimer****:*

*The development for this processor has begun as of December, 24th, 2024. Documentation for it began January 4th, 2025. The information provided in this overview is subject to change until the processor architecture is fully assembled and tested. A less formal report will be available alongside this one. That report will include prototype information and branching ideas that will lead to the architecture described here for the G2X8.*

The G2X8 is the latest iteration on a line of CPUs developed by Edward Gonell. The previous rendition was the G400, a four-bit CPU with a simple instruction set. The previous CPU required a single clock cycle to execute one instruction; however, it came at the cost of accessing memory for every instruction executed. This rendition of our CPU architecture is more akin to a CISC CPU than the previous one. This CPU hosts a robust Fetch pipeline with the capability of addressing up to 64k words. A Decoder that assembles variable length instructions. Smart Scheduler with dedicated or standalone resource allocation, and token generation. Also, three execution units, two Arithmetic and one Memory Management Unit. To tie all the instructions together with their destinations a Stack is implemented. Not less important a bank of sixteen, two-word registers are available to the end user.

*Fig. 1 - General overview of the processor layout.*

EU0

Control Unit

ALU 8

Reg B88

Reg B8

Reg C88

Reg C8

Reg D8

B8

Reg D8

Reg E8

Reg E8

ACC8

ACC8

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